IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A semiconductor memory device having a gate electrode and a diffusion layer, comprising:

a plurality of memory cells each of which including the gate electrode and the diffusion layers;

a first contact layer connected to one of the diffusion layer of the memory cell;

a second contact layer connected to the first contact layer;

a bit line connected to the second contact layer; and

a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being same as a height of the first contact layer.

2. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 1, the first contact layer includes a W layer.

3. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 1, comprising the first contact layer including a first conductive film and a second conductive film.

4. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 3, the first conductive film is Ti.

5. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 3, the second conductive film is W.

6. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 1, the semiconductor memory device is one of a NAND type nonvolatile memory device and a NOR type memory device.

7. (Original) A memory card including the semiconductor memory device recited in claim 1.

8. (Original) A card holder to which the memory card recited in claim 7 is inserted.

9. (Original) A connecting device to which the memory card recited in claim 7 is inserted.

10. (Original) The connecting device according to the claim 9, the connecting device is configured to be connected to a computer.

11. (Original) A memory card including the semiconductor memory device recited in claim 1 and a controller which controls the semiconductor memory device.

12. (Original) A card holder to which the memory card recited in claim 11 is inserted.

13. (Original) A connecting device to which the memory card recited in claim 11 is inserted.

14. (Original) The connecting device according to the claim 13, the connecting device is configured to be connected to a computer.

15 (Original) An IC card on which an IC chip that includes the semiconductor memory device recited in claim 1 is located.

16. (Original) A semiconductor memory device having a gate electrode and a diffusion layer, comprising:

a plurality of memory cells each of which including the gate electrode and the diffusion layer;

an insulating film formed above side and top surfaces of the gate electrode of the semiconductor memory device;

a first interlayer insulating layer formed between the gate electrode of the semiconductor memory device;

a first contact layer formed in the first interlayer insulating layer and connected to the diffusion layer;

a second interlayer insulting layer formed on the first inter layer insulating layer ;

a second contact layer formed in the second interlayer insulating layer and connected to the first contact layer;

a bit line connected to the second contact layer; and

a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers

being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being same as a height of the first contact layer.

17. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 1, the first contact layer includes a W layer.

18. (Currently Amended) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, a position of a top surface of the [[insulting]] insulating film formed above the gate electrode of the semiconductor memory device is same as that of the top surface of the first interlayer insulating layer.

19. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, a position of a top surface of the insulting film formed above the gate electrode of the semiconductor memory device is different from that of the top surface of the first interlayer insulating layer.

20. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, the conductive layer is a source line.

21. (Original) The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, the semiconductor memory device is one of a NAND type nonvolatile memory device and a NOR type memory device.

22. (Original) A memory card including the semiconductor memory device recited in claim 16.

23. (Original) A card holder to which the memory card recited in claim 22 is inserted.

24. (Original) A connecting device to which the memory card recited in claim 22 is inserted.

25. (Original) The connecting device according to the claim 24, the connecting device is configured to be connected to a computer.

26. (Original) A memory card including the semiconductor memory device recited in claim 16 and a controller which controls the semiconductor memory device.

27. (Original) A card holder to which the memory card recited in claim 26 is inserted.

28. (Original) A connecting device to which the memory card recited in claim 26 is inserted.

29. (Original) The connecting device according to the claim 28, the connecting device is configured to be connected to a computer.

30. (Currently Amended) An IC card on which an IC chip that includes the semiconductor memory device recited in claim 26 [[1]] is located.

31-46. (Canceled)